What is claimed is:

1. A memory device, comprising:

a NOR architecture floating gate memory array formed on a substrate having a plurality of pillars and associated intervening trenches; and

a plurality of memory cell structures, each memory cell structure comprising,

a floating gate memory cell, wherein the floating gate memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the floating gate memory cell by a source and drain region formed at the bottom of the trench.

2. The memory device of claim 1, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of the floating gate memory cells of the plurality of memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of memory cell structures;

at least one bitline, wherein the at least one bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

at least one source line, wherein the at least one source line is coupled to one or more floating gate memory cell source regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

3. The memory device of claim 2, wherein the plurality of memory cell structures are formed into rows and columns such that each trench contains a memory cell structure and where the floating gate memory cell and select gate of each memory cell structures of each row are arranged in an alternating pattern, such

that each pillar of the row has either two select gates or two floating gate memory cells formed on opposing sidewalls.

4. A floating gate memory cell structure, comprising:
a substrate, comprising two raised areas, defining a trench therebetween;
a floating gate memory cell, wherein the floating gate memory cell is formed vertically on a first sidewall of the trench;
a select gate memory cell, wherein the select gate is formed vertically on a second sidewall of the trench; and
wherein the floating gate memory cell is coupled to the select gate by source and drain region formed at the bottom of the trench.

5. The floating gate memory cell structure of claim 4, wherein the raised areas are pillars.

6. The floating gate memory cell structure of claim 4, further comprising:
a word line, wherein the word line is coupled to a control gate of the floating gate memory cell of the floating gate memory cell structure;
a select line, wherein the select line is coupled to a control gate of the select gate of the floating gate memory cell structure;
a bitline, wherein the bitline is coupled to a drain of the select gate; and
a source line, wherein the source line is coupled to a source of the floating gate memory cell.

7. A floating gate memory array, comprising:
a substrate, comprising a plurality of pillars and associated intervening trenches; and
a plurality of memory cell structures, each memory cell structure comprising,
a floating gate memory cell, wherein the floating gate memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the floating gate memory cell by a source and drain region formed at the bottom of the trench.

8. The floating gate memory array of claim 7, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of the floating gate memory cells of the plurality of memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of memory cell structures;

at least one bitline, wherein the at least one bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

at least one source line, wherein the at least one source line is coupled to one or more floating gate memory cell source regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

9. The floating gate memory array of claim 8, wherein the plurality of memory cell structures are formed into rows and columns such that each trench contains a memory cell structure and where the floating gate memory cell and select gate of each memory cell structure of each row are arranged in an alternating pattern, such that each pillar of the row has either two select gates or two floating gate memory cells formed on opposing sidewalls.

10. The floating gate memory array of claim 7, wherein the plurality of memory cell structures are formed into rows and columns and an isolation region is formed between adjacent rows of memory cell structures of the plurality of memory cell structures.

11. The floating gate memory array of claim 10, wherein the isolation region is an

oxide insulator.

12. The floating gate memory array of claim 7, wherein the plurality of memory cell structures are formed into rows and columns and each row of memory cell structures is formed on a separate P-well isolation region formed on the substrate.

13. A memory device comprising:

a NOR architecture floating gate memory array formed on a substrate having a plurality of pillars and associated intervening trenches;

a plurality of memory cell structures, each memory cell structure comprising,

a floating gate memory cell, wherein the floating gate memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the floating gate memory cell by a source and drain region formed at the bottom of the trench;

a control circuit;

a row decoder;

a plurality of word lines, wherein each word line is coupled to one or more control gates of the floating gate memory cells of the plurality of memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of memory cell structures;

at least one bitline, wherein the at least one bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

at least one source line, wherein the at least one source line is coupled to one or more floating gate memory cell source regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

14. A system, comprising:

a processor coupled to at least one memory device, wherein the at least one memory device comprises,

a NOR architecture floating gate memory array formed on a substrate having a plurality of pillars and associated intervening trenches, and

a plurality of memory cell structures, each memory cell structure comprising,

a floating gate memory cell, wherein the floating gate memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the floating gate memory cell by a source/drain region formed at the bottom of the trench.

15. A method of forming a floating gate memory cell structure, comprising:

forming two raised areas on a substrate, the raised areas defining an associated intervening trench;

forming a floating gate memory cell on a first sidewall of the trench;

forming a select gate on a second sidewall of the trench; and

forming a source and drain region at the bottom of the associated intervening trench.

16. The method of claim 15, wherein forming two raised areas on a substrate further comprises etching a trench in the substrate.

17. The method of claim 15, wherein forming two raised areas on a substrate further comprises forming two pillars on a substrate.

18. The method of claim 17, wherein forming two pillars on a substrate further comprises depositing additional substrate material on the substrate to form the two pillars.

19. The method of claim 15, wherein forming a source and drain region at the bottom of the associated intervening trench further comprises forming source and drain regions on the top of the two raised areas and at the bottom of the associated intervening trench in one of before the formation of the floating gate memory cell and select gate and after the formation of the floating gate memory cell and select gate.

20. The method of claim 15, wherein the substrate is P-doped.

21. The method of claim 15, wherein forming a floating gate memory cell on a first sidewall of the trench and forming a select gate on a second sidewall of the trench further comprises forming a floating gate transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall.

22. The method of claim 21, wherein forming a floating gate transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall further comprises forming a tunnel insulator on the surface of the first sidewall, forming a floating gate on the tunnel insulator, forming a first insulator as an intergate/interpoly insulator over the floating gate, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator.

23. The method of claim 22, wherein forming a tunnel insulator on the surface of the first sidewall, forming a floating gate on the tunnel insulator, forming a first

insulator as an intergate/interpoly insulator over the floating gate, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a floating gate on the tunnel insulator, then forming the first and second insulators over the floating gate and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the two raised areas and trench, masked, and directionally etched.

24. A method of forming a floating gate memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; and

forming a plurality of floating gate memory cell structures, each floating gate memory cell structure having a floating gate and a coupled select gate, where each floating gate memory cell structure is formed by,

depositing a layer of tunnel insulator material over two pillars and an intervening trench;

masking and anisotropically etching the layer of tunnel insulator material to form a tunnel insulator of a floating gate memory cell on a first sidewall of the trench;

depositing a layer of floating gate material over the two pillars and intervening trench;

masking and anisotropically etching the layer of floating gate material to form a floating gate on the tunnel insulator on the first sidewall of the trench;

depositing a layer of gate insulator material over the two pillars and intervening trench;

masking and anisotropically etching the layer of gate insulator material to

form a first gate insulator on the floating gate on the first sidewall and a second gate insulator of a select gate on a second sidewall of the trench;

depositing a layer of gate material over the two pillars and intervening trench;

masking and anisotropically etching the layer of gate material to form a first and second control gates on the first and second gate insulators on the first and second sidewalls of the trench; and

diffusing a dopant material into the bottom of the trench and the tops of the two pillars to form source regions and drain regions of the select gate and the floating gate memory cell.

25. The method of claim 24, further comprising:

forming the plurality of floating gate memory cell structures into rows; and

forming an isolation region between adjacent rows of floating gate memory cell structures by depositing an oxide insulator between adjacent rows.

26. A method of forming a NOR architecture floating gate memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate; and

forming a plurality of floating gate memory cell structures, each floating gate memory cell structure formed by,

forming a floating gate memory cell on a first sidewall of a trench;

forming a select gate on a second sidewall of the trench; and

forming a source/drain region at the bottom of the trench.

27. The method of claim 26, wherein the substrate is P-doped.

28. The method of claim 26, further comprising:

forming the plurality of floating gate memory cell structures into rows; and

forming a P-well isolation region under each row of floating gate memory cell structures.

29. The method of claim 26, further comprising:
forming the plurality of floating gate memory cell structures into rows; and
forming an isolation region between adjacent rows of floating gate memory cell structures.

30. The method of claim 29, wherein forming an isolation region between adjacent rows of floating gate memory cell structures further comprises forming an isolation region of an oxide insulator.

31. The method of claim 29, further comprising:
forming a plurality of word lines across the isolation region between adjacent rows of floating gate memory cell structures, wherein each word line is coupled to a control gate of a single floating gate memory cell of each row of floating gate memory cell structures.

32. The method of claim 29, further comprising:
forming a plurality of select lines across the isolation region between adjacent rows of floating gate memory cell structures, wherein each select line is coupled to a control gate of a single select gate of each row of floating gate memory cell structures.

33. The method of claim 26, wherein forming a floating gate memory cell on a first sidewall of the trench and forming a select gate on a second sidewall of the trench further comprises forming a floating gate transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall.

34. The method of claim 33, wherein forming a floating gate transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall further comprises forming a tunnel insulator on the surface of the first sidewall, forming a floating gate on the tunnel insulator, forming a first insulator as an intergate/interpoly insulator over the floating gate, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator.

35. The method of claim 34, wherein forming a tunnel insulator on the surface of the first sidewall, forming a floating gate on the tunnel insulator, forming a first insulator as an intergate/interpoly insulator over the floating gate, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a floating gate on the tunnel insulator, then forming the first and second insulators over the floating gate and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the trench, masked, and directionally etched in combined layers to produce the floating gate and select gate gate-insulator stacks.

36. The method of claim 26, further comprising:

forming at least one bitline, wherein the at least one bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

forming at least one source line, wherein the at least one source line is coupled to one or more floating gate memory cell source regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

37. The method of claim 26, wherein forming a plurality of floating gate memory cell structures further comprises forming a plurality of floating gate memory cell structures, wherein the plurality of memory cell structures are formed into rows and where the floating gate memory cell and select gate of each memory cell structure of each row are formed in an alternating pattern, such that each pillar of the row has either two select gates or two floating gate memory cells formed on its sidewalls.

38. A method of forming an EEPROM memory device, comprising:
forming a plurality of pillars and associated intervening trenches on a substrate;
forming a plurality of vertical floating gate memory cells on a first sidewall of each trench;
forming a plurality of vertical select gates on a second sidewall of each trench; and
forming one or more source/drain regions at the bottom of the associated intervening trenches and one or more source or drain regions on the top of the plurality of pillars.

39. A NAND architecture floating gate memory cell string, comprising:
a substrate, comprising two or more raised areas, defining trenches therebetween;
a plurality of floating gate memory cells, wherein the floating gate memory cells are formed vertically on the sidewalls of the trenches;
wherein the plurality of floating gate memory cells are coupled in a serial string by source/drain regions formed at the top of the two or more raised areas and at the bottom of the one or more trenches; and
wherein a first floating gate memory cell is coupled to a first select gate, where the first select gate is formed vertically on a sidewall of a selected trench.

40. The NAND architecture floating gate memory cell string of claim 39, wherein a

last floating gate memory cell is coupled to a second select gate, where the second select gate is formed vertically on a sidewall of a second selected trench.

41. The NAND architecture floating gate memory cell string of claim 39, wherein the raised areas are pillars.

42. The NAND architecture floating gate memory cell string of claim 41, further comprising:

a plurality of word lines, wherein each word line is coupled to a control gate of a floating gate memory cell of the string;

a plurality of select lines, wherein each select line is coupled to a control gate of a select gate of the string;

a bitline, wherein the bitline is coupled to a drain of the first select gate; and

a source line, wherein the source line is coupled to a source of the second select gate of the string.

43. A NAND architecture memory array, comprising:

a substrate, comprising a plurality of pillars and associated intervening trenches;

a plurality of floating gate memory cells, wherein the floating gate memory cells are formed vertically on the sidewalls of the plurality of pillars and trenches, wherein the plurality of floating gate memory cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches, and where a first floating gate memory cell of each string is coupled to a first vertical select gate and a last floating gate memory cell of each string is coupled to a second vertical select gate

a plurality of word lines, wherein each word line is coupled to one or more control gates of one or more floating gate memory cells, where each of the one or more floating gate memory cells is from a differing string of the plurality of NAND architecture memory strings;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one bitline, wherein the at least one bitline is coupled to a drain of the first select gate of each string of the plurality of NAND architecture memory strings; and

at least one source line, wherein the at least one source line is coupled to a source of the second select gate of each string of the plurality of NAND architecture memory strings.

44. The NAND architecture memory array of claim 43, wherein an isolation region is formed between adjacent strings of the plurality of NAND architecture memory strings.

45. A memory device comprising:

a NAND architecture memory array formed on a substrate having a plurality of pillars and associated intervening trenches;

a plurality of floating gate memory cells, wherein the floating gate memory cells are formed vertically on the sidewalls of the plurality of pillars and trenches;

wherein the plurality of floating gate memory cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches;

wherein a first floating gate memory cell of each string is coupled to a first vertical select gate and a last floating gate memory cell of each NAND architecture memory string is coupled to a second vertical select gate;

a control circuit;

a row decoder;

a plurality of word lines coupled to the row decoder, wherein each word line is coupled to one or more control gates of one or more floating gate memory cells, where each of the one or more floating gate memory cells is from a

differing string of the plurality of NAND architecture memory strings;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one bitline, wherein the at least one bitline is coupled to a drain of the first select gate of each string of the plurality of NAND architecture memory strings; and

at least one source line, wherein the at least one source line is coupled to a source of the second select gate of each string of the plurality of NAND architecture memory strings.

46. The memory device of claim 45, wherein memory device is a EEPROM memory device.

47. A system, comprising:

a processor coupled to at least one memory device, wherein the at least one memory device comprises,

a NAND architecture memory array formed on a substrate having a plurality of pillars and associated intervening trenches,

a plurality of floating gate memory cells, wherein the floating gate memory cells are formed vertically on the sidewalls of the plurality of pillars and trenches,

wherein the plurality of floating gate cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches, and

wherein a first floating gate memory cell of each string is coupled to a first vertical select gate and a last floating gate memory cell of each NAND architecture memory string is coupled to a second vertical select gate.

48. A memory device comprising:

a NAND architecture memory array formed on a substrate having a plurality of floating gate memory cells arranged in rows and columns and coupled into a plurality of NAND memory strings, wherein the floating gate memory cells are formed vertically on the sidewalls of the plurality of pillars and associated trenches formed on the substrate, and where the plurality of floating gate cells are coupled into the plurality of NAND memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches;

wherein a first floating gate memory cell of each string is coupled to a first vertical select gate and a last floating gate memory cell of each string is coupled to a second vertical select gate;

a plurality of word lines, wherein each word line is coupled to one or more gates of a row of the floating gate memory cells;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one bitline, wherein the at least one bitline is coupled to a drain of the first select gate of each string of the plurality of NAND architecture memory strings; and

at least one source line, wherein the at least one source line is coupled to a source of the second select gate of each string of the plurality of NAND architecture memory strings.

49. A method of forming a NAND architecture memory cell string, comprising:

forming one or more raised areas on a substrate, the raised areas defining associated intervening trenches;

forming a plurality of floating gate memory cells on the sidewalls of the one or more raised areas;

forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches; and

forming a first vertical select gate coupled to a first floating gate memory cell of the NAND architecture memory string and a second vertical select gate coupled to a last floating gate memory cell of the NAND architecture memory string.

50. The method of claim 49, wherein forming one or more raised areas on a substrate further comprises etching a trench in the substrate.

51. The method of claim 49, wherein forming one or more raised areas on a substrate further comprises forming one or more pillars on a substrate.

52. The method of claim 51, wherein forming one or more raised areas on a substrate further comprises depositing additional substrate material on the substrate to form the one or more pillars.

53. The method of claim 49, wherein forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches further comprises forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches in one of before the formation of the plurality of floating gate memory cells and after the formation of the plurality of floating gate memory cells.

54. The method of claim 49, wherein forming a plurality of floating gate memory cells on the sidewalls of the one or more raised areas and forming a first vertical select gate coupled to a first floating gate memory cell of the NAND architecture memory string and a second vertical select gate coupled to a last floating gate memory cell of the NAND architecture memory string further comprises forming a plurality of floating gate memory cells on the sidewalls of the one or more raised areas by forming a floating gate gate-insulator stack on

the surface of a first plurality of selected sidewalls and forming a first and second vertical select gate gate-insulator stack on the surface of a second plurality of selected sidewalls.

55. The method of claim 54, wherein forming a plurality of floating gate memory cells on the sidewalls of the one or more raised areas by forming a floating gate gate-insulator stack on the surface of a first plurality of selected sidewalls and forming a first and second vertical select gate gate-insulator stack on the surface of a second plurality of selected sidewalls further comprises forming a tunnel insulator on the surface of the first plurality of selected sidewalls, forming a floating gate on the tunnel insulator, forming a first insulator as an intergate/interpoly insulator over the floating gate, and forming a first control gate over the first insulator, and on the surface of the second plurality of selected sidewalls forming a second insulator and forming a second control gate over the second insulator.

56. The method of claim 55, wherein forming a tunnel insulator on the surface of the first plurality of selected sidewalls, forming a floating gate on the tunnel insulator, forming a first insulator as an intergate/interpoly insulator over the floating gate, and forming a first control gate over the first insulator, and on the surface of the second plurality of sidewalls forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first plurality of selected sidewalls and forming a floating gate on the tunnel insulator, then forming the first and second insulator over the floating gate of the first plurality of selected sidewalls and on the surface of the second plurality of selected sidewalls, and forming the first and second control gate over the first and second insulator, wherein each layer is deposited over the two raised areas and trench, masked, and directionally etched.

57. A method of forming a NAND architecture memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate;

forming a plurality of vertical floating gate memory cells on a first plurality of selected sidewalls of the plurality of pillars;

forming a plurality of select gates on a second plurality of selected sidewalls of the plurality of pillars; and

forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches to form a plurality of NAND architecture memory strings.

58. The method of claim 57, further comprising:

forming a P-well isolation region under each NAND architecture memory string.

59. The method of claim 57, further comprising:

forming an isolation region between adjacent NAND architecture memory strings.

60. The method of claim 59, further comprising:

forming a plurality of word lines and a plurality of select lines across the isolation region between adjacent NAND architecture memory strings, wherein each word line is coupled to a control gate of a single floating gate memory cell of each NAND architecture memory string and each select line is coupled to a select gate of each NAND architecture memory string.

61. The method of claim 57, wherein forming a plurality of vertical floating gate memory cells on the first plurality of selected sidewalls and forming a plurality of select gates on a second plurality of selected sidewalls further comprises forming a floating gate gate-insulator stack on the surface of the first plurality of selected sidewalls and forming a select gate gate-insulator stack on the surface of the second plurality of selected sidewalls.

62. The method of claim 61, wherein forming a floating gate gate-insulator stack on the surface of the first plurality of selected sidewalls and forming a select gate gate-insulator stack on the surface of the second plurality of selected sidewalls further comprises forming a tunnel insulator on the surface of the first plurality of selected sidewalls, forming a floating gate on the tunnel insulator, forming an intergate/interpoly insulator over the floating gate, and forming a control gate over the intergate/interpoly insulator and forming an insulator on the surface of the second plurality of selected sidewalls and forming a control gate over the insulator.

63. A method of forming a memory device, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate;

forming a plurality of vertical floating gate memory cells on a first plurality of selected sidewalls of the plurality of pillars;

forming a plurality of select gates on a second plurality of selected sidewalls of the plurality of pillars; and

forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches to form a plurality of NAND architecture memory strings.

64. A method of forming a NAND architecture floating gate memory cell string, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; and

forming a NAND architecture floating gate memory cell string having a plurality of floating gates and one or more select gates, where the string is formed by,

depositing a layer of tunnel insulator material over the plurality of pillars and

intervening trenches;

masking and anisotropically etching the layer of tunnel insulator material to form a tunnel insulator of a floating gate memory cell on a first selected number of sidewalls of the pillars;

depositing a layer of floating gate material over the plurality of pillars and intervening trenches;

masking and anisotropically etching the layer of floating gate material to form a floating gate on the tunnel insulator on the first selected number of sidewalls;

depositing a layer of gate insulator material over the plurality of pillars and intervening trenches;

masking and anisotropically etching the layer of gate insulator material to form a gate insulator on the floating gate on the first selected number of sidewalls and gate insulator of a select gate on a second selected number of sidewalls of the pillars;

depositing a layer of gate material over the plurality of pillars and intervening trenches; and

masking and anisotropically etching the layer of gate material to form a control gate on the gate insulator material the first and second selected numbers of sidewalls.

65. The method of claim 64, further comprising:

diffusing a dopant material into the bottom of each trench and the top of each pillar to form source regions and drain regions of the one or more select gates and the plurality of floating gate memory cells.